WHAT IS CLAIMED IS:

1. A data routing unit comprising:

a data receiver;

a data transmitter; and

a bridge circuit connected to supply data to said data receiver and to receive data from said data transmitter, said bridge circuit connected to at least one set of data input lines and at least one set of data output lines, said bridge circuit responsive to a header of a data packet received from said data transmitter or received from said at least one set of data input lines to selectively route said received data packet to (1) said data receiver circuit, (2) a selected set of said at least one data output lines, or (3) both said data receiver circuit and a selected set of said at least one set of data output lines dependent upon said header.

2. The data routing unit of claim 1, further comprising:

an input/output memory connected to said data receiver for storing data received by said data receiver and to said data transmitter for storing data to be transmitted by said data transmitter.

3. The data routing unit of claim 2, further comprising:

a central processing unit connected said input/output memory for storing data into said input/output memory and reading data from said input/output memory.

4. The data routing unit of claim 1, wherein:

said at least one set of data input lines consists of a right set of data input lines and a left set of data input lines; and

said at least one set of data output lines consists of a right set of data output lines and a left set of data input lines.

5. The data routing unit of claim 1, wherein:

each of said at least one set of data output lines consists of a plurality of data lines and a data routing unit clock line; and

said data transmitter generating data transmitted on said data lines synchronous with a transmitter clock signal on said data routing unit clock line.

6. The data routing unit of claim 5, further comprising:

an input/output memory connected to said data receiver for storing data received by said data receiver and to said data transmitter for storing data to be transmitted by said data transmitter; and

a central processing unit connected said input/output memory for storing data into said input/output memory and reading data from said input/output memory, said central processing unit operating in synchronism with a CPU clock which is asynchronous with said transmitter clock signal.

7. The data routing unit of claim 1, wherein:

each of said at least one set of data input lines consists of a plurality of data lines and a data routing unit clock line; and

said data receiver sensing data received on said data lines synchronous with a transmitter clock signal on said data routing unit clock line.

8. The data routing unit of claim 7, further comprising:

an input/output memory connected to said data receiver for storing data received by said data receiver and to said data transmitter for storing data to be transmitted by said data transmitter; and

a central processing unit connected said input/output memory for storing data into said input/output memory and reading data from said input/output memory, said central processing unit operating in synchronism with a CPU clock which is asynchronous with said transmitter clock signal.

9. The data routing unit of claim 1, wherein:

said bridge circuit further includes

a node address register storing a uniquely assigned multibit node address;

a node address comparator connected to said node address register for comparing predetermined destination node address bits of said header with said node address stored in said node address register; and

said bridge circuit selectively routing said received data packet to said data receiver when said destination node address bits matches said node address.

10. The data routing unit of claim 9, wherein:

said bridge circuit further includes

a plurality of routing registers, each routing register corresponding to one set of data output lines, each routing register storing an indication of a set of node addresses;

a plurality of routing comparators, each routing comparator connected to a corresponding routing register for comparing predetermined destination node address bits of said header with said indication of as set of node addresses stored in said corresponding routing register; and

said bridge circuit selectively routing said received data packet to a set of data output lines when said destination node address bits matches a node address of said set of node addresses stored in said corresponding routing register.

11. The data routing unit of claim 9, wherein:

said at least one set of data input lines consists of a right set of data input lines and a left set of data input lines;

said at least one set of data output lines consists of a right set of data output lines and a left set of data input lines;

said bridge circuit further includes

a right routing register storing a right routing data word having a plurality of bits, each bit corresponding to a unique node address and having either

a first digital state indicating routing via said right data output lines to reach said unique node address or a second digital state indicating not routing via said right data output lines to reach said unique node address;

a left routing register storing a left routing data word having a plurality of bits, each bit corresponding to a unique node address and having either a first digital state indicating routing via said left data output lines to reach said unique node address or a second digital state indicating not routing via said left data output lines to reach said unique node address;

a decoder receiving said header for converting said destination node address into a multibit destination data word having a bit corresponding to said destination node address in said first digital state and all other bits in said second digital state;

a right comparator connected to said right routing register and said decoder for comparing said right routing data word and said destination data word; and

a left comparator connected to said left routing register and said decoder for comparing said left routing data word and said destination data word; and

said bridge circuit selectively routing said received data packet to said right data output lines when said destination data word matches said right routing data word and selectively routing said received data packet to said left data output lines when said destination data word matches said left routing data word.

12. The data routing unit of claim 11, further comprising:

an input/output memory connected to said data receiver for storing data received by said data receiver and to said data transmitter for storing data to be transmitted by said data transmitter; and

a central processing unit connected said input/output memory for storing data into said input/output memory and reading data from said input/output memory, said central processing unit operable to write data into said right routing register and into said left routing register.

13. The data routing unit of claim 1, wherein:

said at least one set of data input lines consists of a right set of data input lines and a left set of data input lines;

said at least one set of data output lines consists of a right set of data output lines and a left set of data input lines;

said bridge circuit selectively routing said received data packet to said data receiver when a predetermined central navigation bit of said header has a first digital state, routing said received data packet with said header deleted to said right set of data output line when a predetermined right navigation bit of said header has said first digital state and routing said received data packet with said header deleted to said left set of data output line when a predetermined left navigation bit of said header has said first digital state.